Display Datasheet

2.1", 132 ppi,

240x146 pixels

Part-No. 800040

Type S021_T1.1

Revision 3

1-Dec-2020

Revision Status	Date	Author	Reason of Modification
1	15-Jan-2018	RN	Initial version
2	07-Jun-2018 11-Sep-2018	AF, RN	Format update Update power consumption values Updated drawing Updated reference connector type Updated power consumption
3	1-Dec-2020	RP	AceP Color

Contents

1. Introduction

1.1 Purpose of this document

This document describes the technical specification of the Plastic Logic 2.1'' color display module (AceP), part number 800040, using the Ultrachip EPD controller/driver UC8156. It defines general characteristics of the display module and the technical information required to integrate the display module into a product.

1.2 Key features of display module

- Consists of an active matrix electrophoretic display which has an integrated EPD controller + source and gate driver IC bonded on the plastic substrate
- Display based on organic TFT active matrix
- 240 x 146 pixels @ 132 ppi
- AceP (Advanced color e-Paper) four colors with red, blue, green, yellow plus black and white
- Full refresh time 15s
- Incorporates industry-leading bi-stable electrophoretic display technology
- Ultra-wide viewing angle
- Enables robust product design
- Flexible
- SPI interface to customer application

1.3 Handling requirements

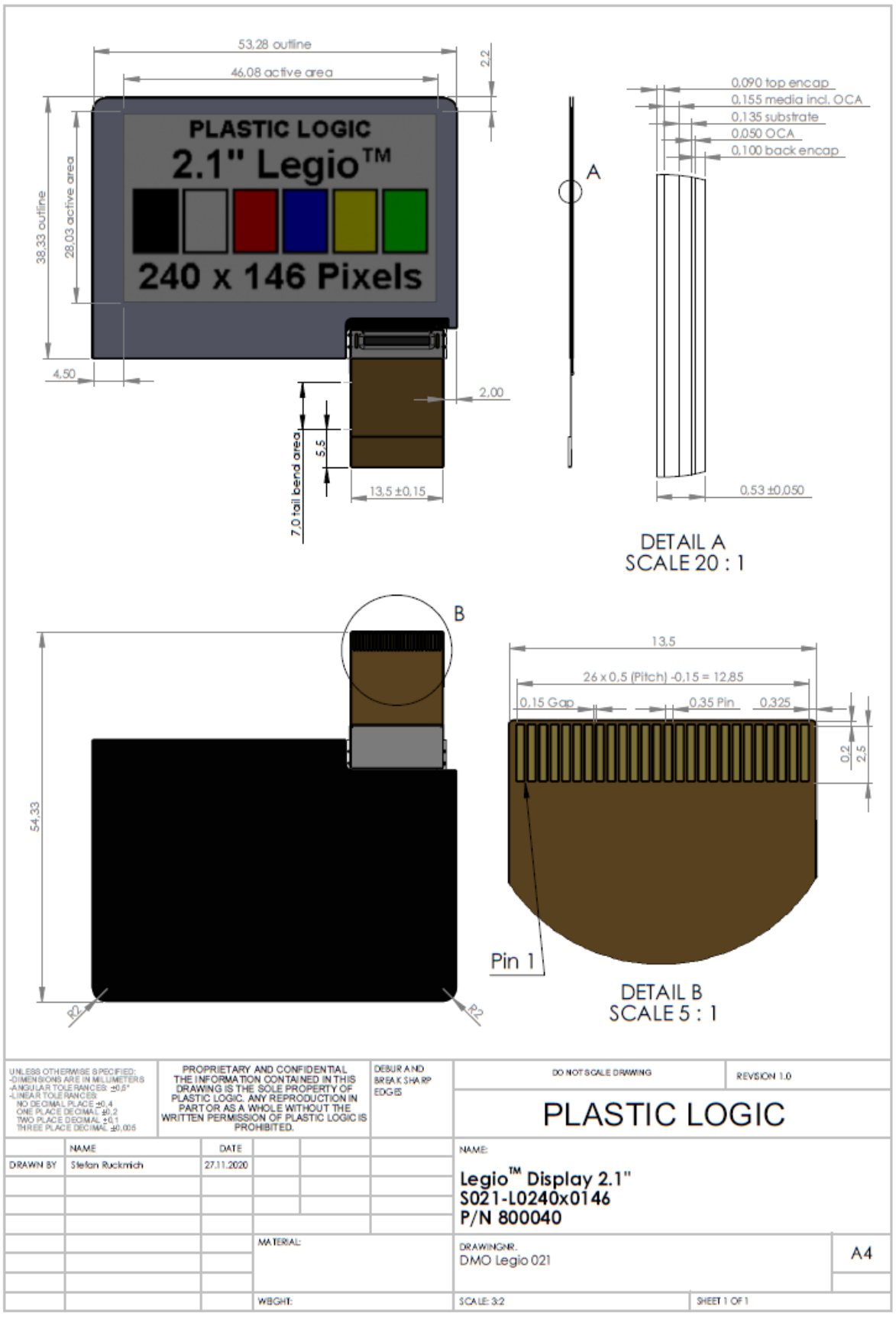
- Please assemble or install the displays in a clean working area.
- Take appropriate care to protect the rear side of the display module from indents and punctures as this may damage the display.
- The display module is an electrostatic discharge (ESD) sensitive device. Ensure proper ESD precautions are in place to avoid damage to the display module. Take care on grounding (e.g. wrist straps) maybe use Ion fans.
- Please handle the display with care during assembly. Do not over-bend and twist the display. Protect especially the COP (chip on plastic) region and the FPC bonding connection.
- Do not connect or disconnect the display from the interface connector while power is on (no "hot-plugging").
- Do not stack the displays.

1.4 General parameters

Parameter	Value	Comments
Module dimensions	52.78 mm x 54.33 mm	Display with FPC connector unfolded
Substrate dimensions	52.78 mm x 40.48 mm	Display without FPC connector
Active screen dimensions	46.08 mm x 28.03 mm	Equivalent to 2.1 inch diagonal
Module thickness	0.53 +/- 0.05mm	Including non-metallic seal
Active screen resolution	240 x 146 pixels	

Parameter	Value	Comments
Active screen pixel pitch	192 µm (square)	Equivalent to approx. 132 ppi, square pixel
Bending radius	30 mm	Active display area
	40 mm	Chip area
Fully integrated EPD controller/driver	UC8156	Bonded to the plastic substrate (COP)
Surface treatment	Anti-glare, UV protection and hard-coat (2H)	

2. Mechanical specification



3. Electrical specification

3.1 Connector interface description

Display connector has 26-pin interface on the FPC, 1-row, with a pitch of 0.5mm.

Pin number	Symbol	Purpose	Function
1,2	VSL	Output	Negative source voltage, connect to capacitor
3,4	VSH	Output	Positive source voltage, connect to capacitor
5,6	VGL	Input	Negative gate voltage, input from booster
7,8	VGH	Input	Positive gate voltage, input from booster
9	GDR_P	Output	P-MOS booster gate control
10	GDR_N	Output	N-MOS booster gate control
11	VDDIO	Power Supply	Interface power connect to VDDA for 3.3V I/O, connect to VDD for 1.8V I/O
12	VDDA	Power Supply	Analog power
13	SPI_MISO	Output	SPI data output
14	SPI_MOSI	Input	SPI data input
15	SPI_CLK	Input	SPI clock
16	SPI_CS	Input	SPI chip select
17	RST_N	Input	Global reset, low active When RST_N becomes low, driver will reset. All registers will be reset to default value and all driver functions will be disabled. SD output and VCOM will base on previous condition; they may have two conditions: 0V or floating.
18	BUSY_N	Output	BUSY pin - indicates the driver status. L: Controller / Driver is busy H: non-busy. Host side can send command/data to driver.
19	GND	Power Supply	Ground
20,21	VDD	Power Supply	Core Logic Power VDD can be regulated internally from VDDA. A capacitor should be connected between VDD and GND.
22	VDDA	Power Supply	Analog power
23	EXTVDD	Input	Controls internal regulator for VDD EXTVDD connected GND: internal regulator is on. EXTVDD connected VDDA: internal regulator is off, need an external 1.8V supply to VDD.
24,25	GND	Power Supply	Ground
26	TPCOM	Output	Connect to capacitor

Note: Refer to the display drawing for Pin1 location.

Reference connector type:

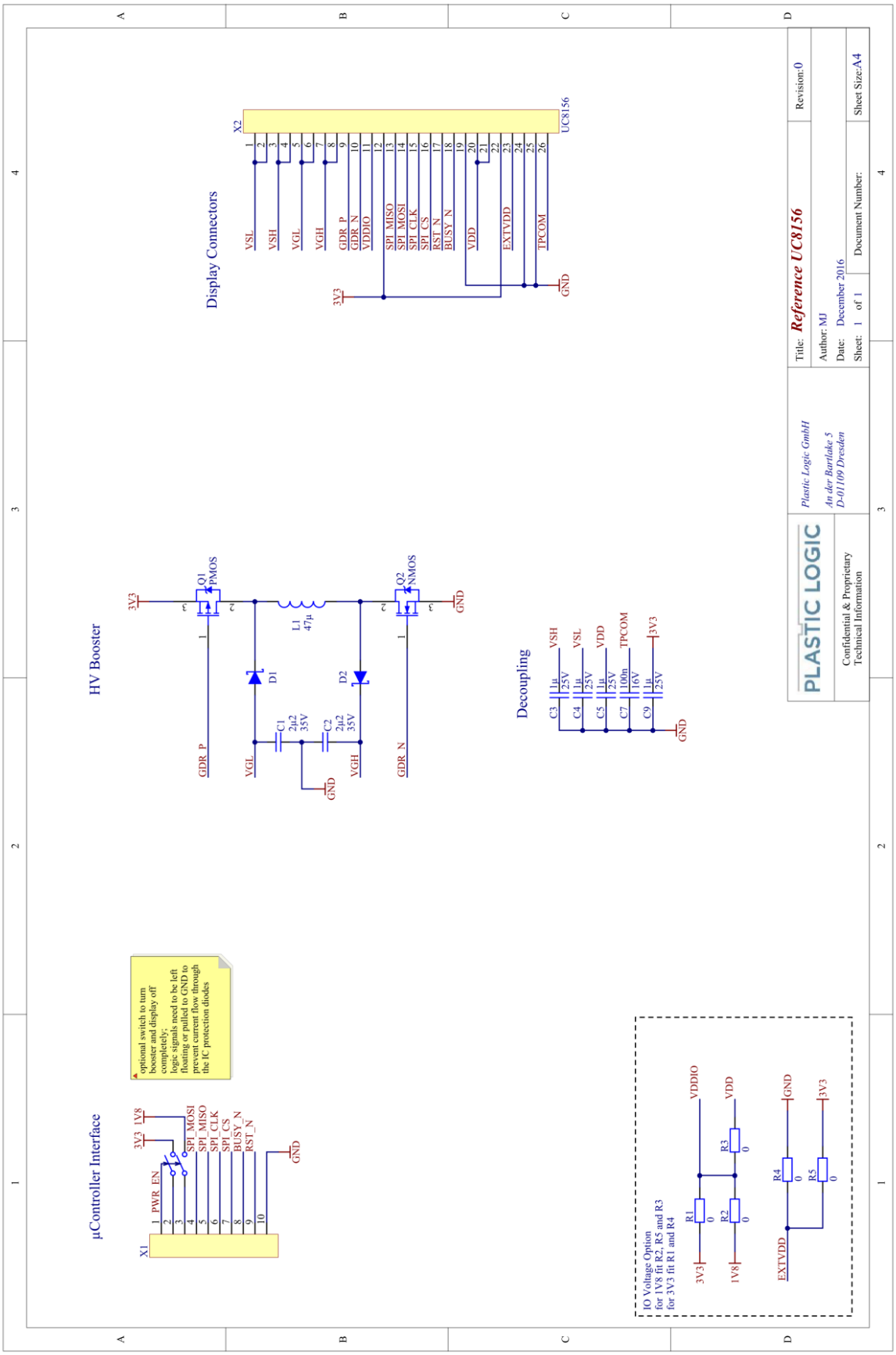
Omron XF2M-2615-1A, 26-pin Rotary Backlock Connector or Hirose FH34SRJ-26S-0.5SH(50), both dual contact, 0.5 mm pitch.

3.2 Controller

The display is driven and controlled by the UC8156 which is an all-in-one EPD driver and timing controller from Ultrachip. This chip is bonded to the Plastic Logic display substrate via a new bonding technology called “Chip on Plastic” (COP).

Please refer to Ultrachip UC8156 datasheet for the full controller specification.

3.3 Application reference circuit



3.4 Display power consumption

Mode	Parameter	Typical	Maximum	Unit
Operation	Mean current for "typical" image update	6		mA
Operation	Mean current for a "worst case" image update	15		mA
Operation	Peak current	160	300	mA
Stand-by with HV's on	Stand-by current 1	4		mA
Stand-by with HV's off	Stand-by current 2	30		µA
Sleep	Sleep current	0.7	0.8	µA

Note (1): see detailed conditions, measurement setup and value calculation below
Note (2): peak current duration ~ 10 µs

Power consumption is very much depending on the finally implemented waveform.

3.4.1 Conditions

1) "Worst case" image = stripe pattern to inverse stripe pattern

Figure 1 – "Worst case" image used for power consumption measurement

3.4.2 Measurement setup

Power consumption specifications were determined by utilizing high side current measurements on the supply power line of the displays. The current rating was detected by measuring the voltage drop over a 0.01 Ohm shunt resistor applying a burden voltage of 10 μ V/mA to the display and sub-sequentially amplifying the signal with an ultra-low offset/drift, low noise precision amplifier. The amplified signal was either detected by an oscilloscope sampling the signal with 2.5 MS/s or a digital multimeter.

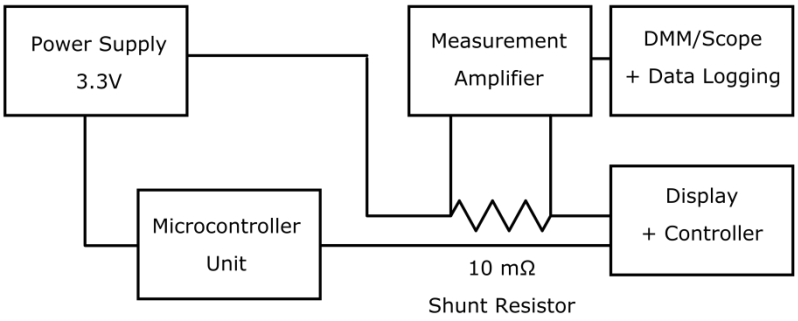


Figure 2 - Measurement Setup

3.4.3 Value calculation for mean power

- The "input current" value is calculated as average value over the whole update (approx. BUSY high time).
- The given value includes the consumption of the display and the complete external display related electronic (HV generation).

4. Safety and Flammability requirements

The integrator of this display module into a final product is responsible for ensuring that the relevant safety and flammability requirements are met.

5. Compatible Evaluation Kits

Do not use any other than the recommended evaluation Kit.