Display Module Datasheet

10.7", colour, 75 ppi, dual edge driven

Part-No. 700259

Revision 3

08-January-2016

Revision Status	Date		Reason of Modification
1	27-Nov-2015		Initial version
2	14-Dec-2015		Release version
3	08-Jan-2016		FPC connector change FPC pin numbering added Pin naming changed Drawing update

Contents

1. Introduction

1.1 Purpose of this document

This document describes the technical specification of the Plastic Logic display module, part number 700259. It defines general characteristics of the display module and the technical information required to integrate the display module into a product.

1.2 Key features of display module

- Organic TFT active matrix
- 640x480 pixels @ 75ppi
- colour
- Incorporates industry-leading bi-stable electrophoretic display technology
- Ultra-wide viewing angle
- Enables robust product design
- Glass free

2. Mechanical specification

2.1 General parameters

Parameter	Value	Unit	Comments
Module dimensions folded	245 x 188	mm	folded state min. dimension
Module thickness	0.65±0.1	mm	active area
Active screen dimensions	217.6±0.17 x 163.2±0.13	mm	equivalent to 271.8 (10.70”) diagonal
Active screen resolution	640x480	pixels	
Pixel pitch	340x340	µm	equivalent to 75ppi.
Sub Pixel resolution	1280x960	pixels	2x2 sub pixels per color pixel
Module mass	37±4	g	
FPC tail minimum internal bend radius	0.7	mm	with E-Z fold design
COF minimum internal bend radius	0.4	mm	bend not permitted at IC location.
Operation temperature	0 to +50	°C	for image update
Storage temperature	-25 to +50	°C	
Operation & storage humidity	15 to 85	%rH	
Top Surface finish hard coat	2	H	Antiglare, UV-protection
Driver Chip Source	2	piece	UC8124
Driver Chip Gate	2	piece	UC8434

Table 1: general specification

2.2 Outline dimensions

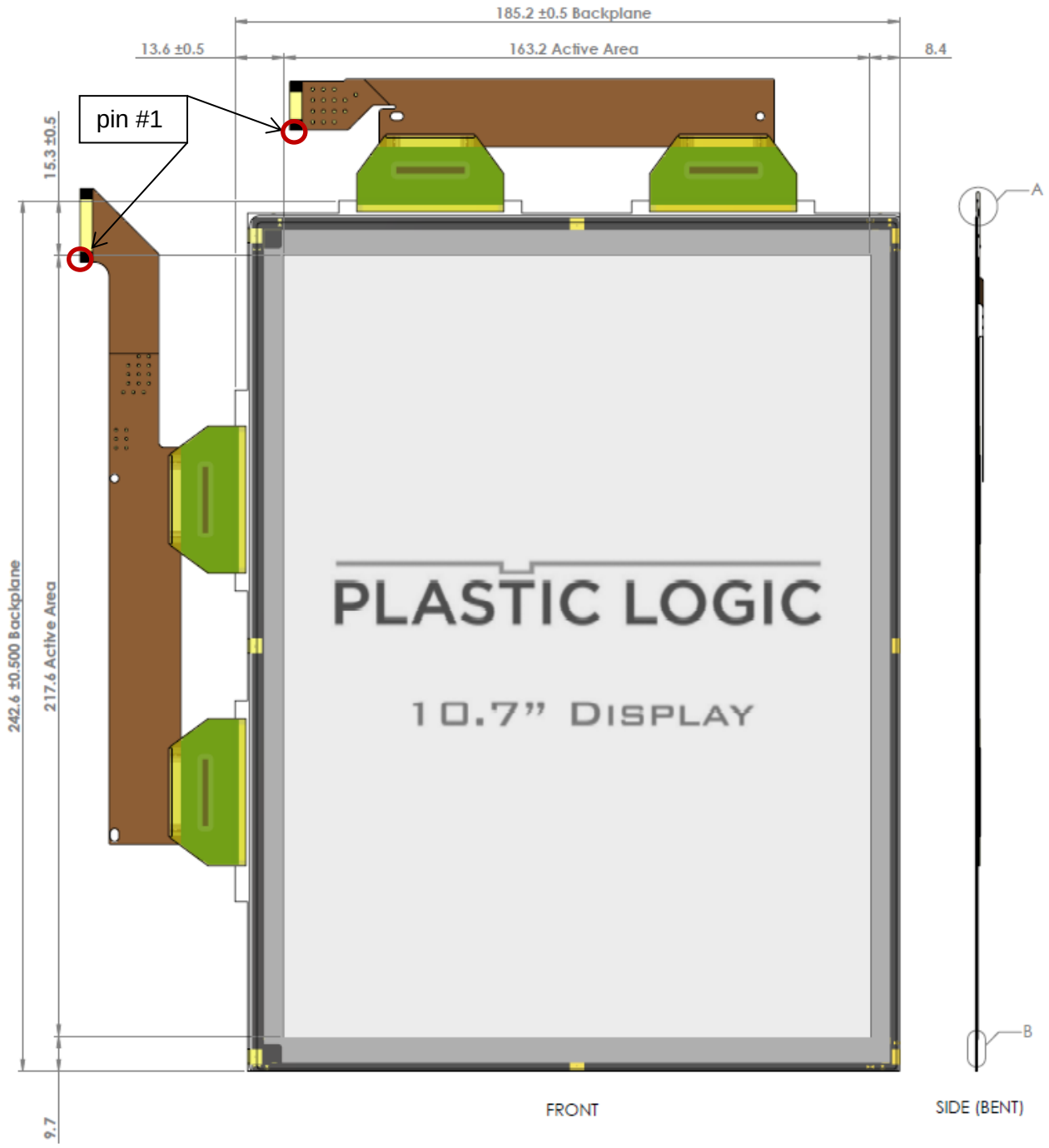

Figure 1: Outline dimension, front side view unfolded state

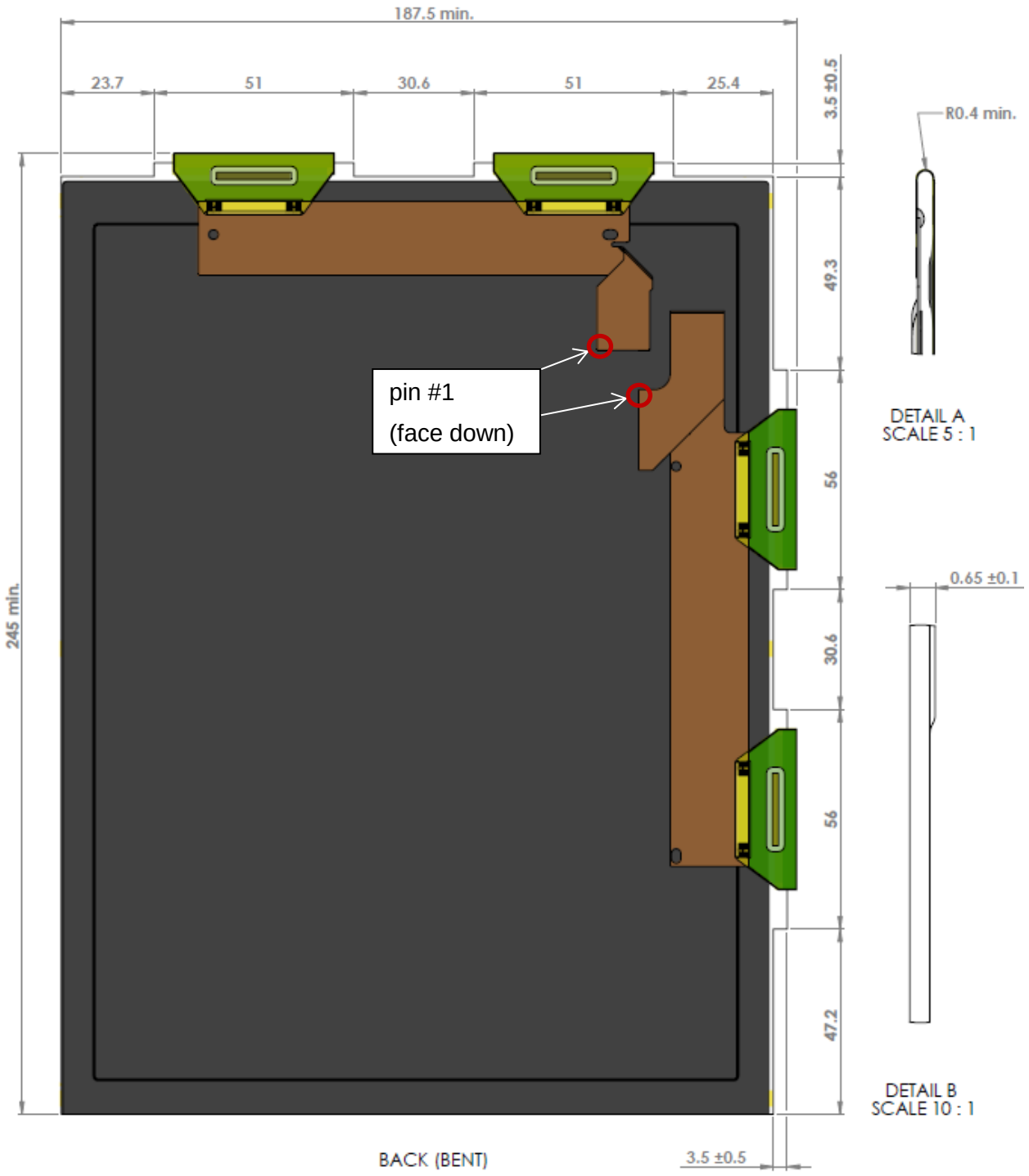

Figure 2: Outline dimensions, backside view folded state

2.3 Colour Filter Array

The colour display uses a RGBW colour filter array positioned directly above the frontplane media surface, aligned with high accuracy to the backplane pixel structure.

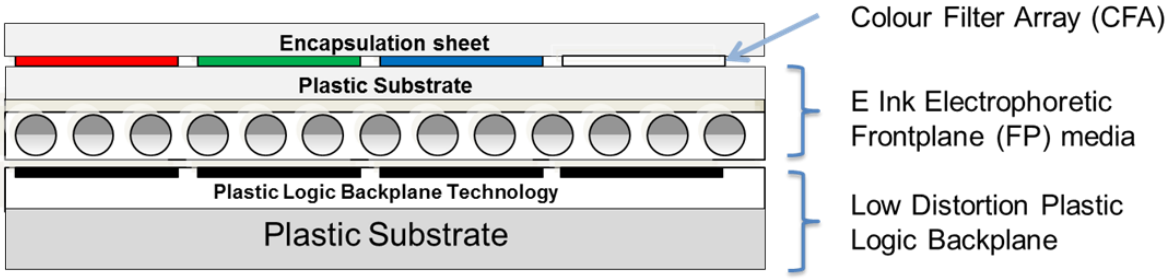

Figure 3: Schematic Layer Stack

The image below gives the arrangement of the sub-pixels in the colour filter which needs to be implemented in the controller settings/software. Primary colours are defined as colours created by driving the sub pixels to black and white only, not using any grey levels.

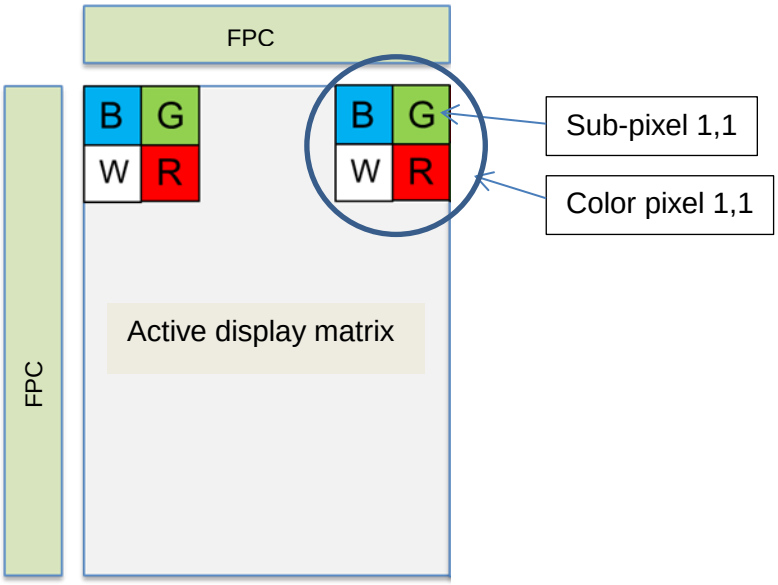

Figure 4: Schematic Layer Stack

3. Optical specification

3.1 Optical requirements

The display supports 4096 color grades.

Grey levels are measured using the L* scale, which is the lightness component of the CIE 1976 CIELUV and CIELAB [2] colour spaces. Measurements in L* can be related to reflectivity using the formula $L^*=116(L/L_w)^{1/3}-16$, where L and L_w are measured in % reflectance and L_w is defined as 100%. This formula is valid for L* > 16.

The following table lists the criteria for the optical inspection of the display module. Inspection shall be done after an image updates with a GC16 waveform using the display specific settings as provided by Plastic Logic (waveform, VCOM, …).

- Viewing Angle : α =±45°
- Viewing Distance : 30cm±10cm
- Ambient Luminance : 700~1000 Lux
- Ambient Temperature : 20°C~25°C
- Ambient Humidity : 40~70%rH

Parameter	Description	Min	Max	Unit
White state	Median white	43	-	L*
Black to White difference	(Median white) – (Median black)	30	-	L*
Contrast ratio	Black to white	8:1		
Colour	NTSC	4.5		%

Table 2: Optical requirements (16GL waveforms)

3.2 Update modes and waveforms

The display module will be supplied with a library of waveforms that are tuned to optimise display performance. Each waveform has an optimum temperature range over which it is valid – it is the responsibility of the display controller and software to ensure that the correct waveform out of the library is selected for the current display module temperature.

Waveforms can be stored in the SPI Flash on the gate FPC. As default SPI Flash is empty but waveform can be pre-programmed on customer request. Waveform format is specific to used EPDC.

The following types of waveform are provided:

Mode Name	Usage	Grey Levels	Ghosting	Update speed
INIT	Recover from unknown state/ start up	White only	Low	Slow
GC16	Full refresh	All colours	Low	Slow
DU	Delta Update; 16GL to Monochrome	All colours → primary colours	High	Medium
A2	Fast monochrome updates	primary colours → primary colours	High	Fast

Notes: Additional customer specific waveforms are possible on request.

Table 3: Waveform types

4. Connectors

4.1 Mechanical

The Display requires two electrical connectors to connect it to the driver electronics.

FPC thickness:	0.3mm ±0.05mm
Connection pitch:	0.5mm
Contact location:	Bottom contact (once tail is folded)
Number of ways:	26 for Gate
	40 for Source

Recommended connectors: HRS FH12-26S-0.5SH & FH12-40S-0.5SH or compatible.

Top contact connector required if connection tails are not folded around.

Note folding the tails reverses the connection order

4.2 Electrical pin-out

Pin	Symbol	Description
1	GND	Ground
2	VCOM	Common voltage
3	VBORDER	Voltage border electrode
4	GD_AD	Active Discharge
5	GD_DIR	Scan Direction
6	VDD	Logic power supply
7	VDD	Logic power supply
8	GD_OE	Mode / Output Enable
9	GND	Ground
10	GD_CLK	Gate Clock
11	GD_SPV2	Shift register start pulse
12	GND	Ground
13	VGH	HV power supply for gate positive
14	VGH	HV power supply for gate positive
15	GND	Ground
16	VGL	HV power supply for gate negative
17	VGL	HV power supply for gate negative
18	GND	Ground
19	SPI_MOSI	SPI Master Out Slave In
20	SPI_CLK	SPI Clock
21	SPI_MISO	SPI Master In Slave Out
22	SPI_CE	SPI Chip Enable
23	GD_SPV1	Shift register start pulse
24	VBORDER	Voltage border electrode
25	VCOM	Common voltage
26	GND	Ground

Table 4: Electrical pin-out for gate FPC

Pin	Symbol	Description
1	VCOM	Common voltage
2	GND	Ground
3	VDD	Logic power supply
4	VDD	Logic power supply
5	GND	Ground
6	VNEG	Negative power supply for driver
7	VNEG	Negative power supply for driver
8	GND	Ground
9	VPOS	Positive power supply for driver
10	VPOS	Positive power supply for driver
11	GND	Ground
12	SD_STL2	Shift register start pulses / Chip Enable
13	SD_ISEL	Input data bus width selection (8 / 16 bit)
14	SD_SHR	Shift Direction
15	SD_OE	Source Output Enable
16	SD_LE	Latch Enable
17	SD_D15	Input Data Line
18	SD_D14	Input Data Line
19	SD_D13	Input Data Line
20	SD_D12	Input Data Line
21	SD_D11	Input Data Line
22	SD_D10	Input Data Line
23	SD_D9	Input Data Line
24	SD_D8	Input Data Line
25	GND	Ground
26	SD_CLK	Source Clock
27	GND	Ground
28	SD_D7	Input Data Line
29	SD_D6	Input Data Line
30	SD_D5	Input Data Line
31	SD_D4	Input Data Line
32	SD_D3	Input Data Line
33	SD_D2	Input Data Line
34	SD_D1	Input Data Line
35	SD_D0	Input Data Line
36	SD_STL1	Shift register start pulses / Chip Enable
37	GND	Ground
38	VBORDER	Voltage border electrode
39	VCOM	Common voltage
40	GND	Ground

Table 5: Electrical pin-out for source FPC

5. Electrical specification

5.1 Absolute maximum ratings

The following table lists the absolute maximum ratings. Exceeding these ratings as well as longer term operation outside the recommended ratings may result in permanent damage of the display module.

Signal	Item	Rating	Unit
VDD	Logic power supply	-0.3~+4.0	V
VGH	HV power supply for gate positive	-0.3~+40	V
VGL	HV power supply for gate negative	-50V~+0.3	V
VGH-VGL	Maximum gate voltage range	80V	V
VPOS	HV power supply for source	-0.3~+18V	V
VNEG	HV power supply for source	-18~+0.3	V
VPOS-VNEG	Maximum source voltage range	36	V

Table 6: Absolute maximum ratings

5.2 DC characteristics

Signal	Parameter	Min	typ	Max	Unit
GND	Signal ground	-	0	-	V
VDD	Logic power supply	3.0	3.3	3.6	V
VGH	HV power supply for gate positive	26	28	30	V
VGL	HV power supply for gate negative	-44	-42	-40	V
VPOS	HV power supply for source positive	14.6	15	15.4	V
VNEG	HV power supply for source negative	-15.4	-15	-14.6	V
VASYM	Asymmetry source (VPOS+VNEG)	-150	0	150	mV
VCOM*	Common voltage	1	5.0	9	V

*VCOM will need to be tuned for each display module. The correct value will be supplied as part of the waveform data.

Table 7: DC characteristics

5.3 Power On/Off Sequence

Power Supply start up sequence

- Initial state: all supplies off (disabled).
- Enable VDD, the source and gate driver logic supplies and allow to stabilize.
- Set SD_OE=0 to set all source outputs to 0V (GND).
- Set GD_OE=0 to set all gate outputs to VGH.
- Open VCOM switch to isolate the display VCOM electrode from the VCOM supply.
- Enable HV supplies in sequence VGH, VCOM, VGL, VNEG, VPOS (see drawing below)
- Allow supplies to stabilize.
- Enable source and gate driver outputs by SD_OE=GD_OE=1.
- Write one null frame to the display.
- Close the VCOM switch.

Display image update

- Write image update data to the display system.
- A final null frame is required as part of the image update (this will be supplied as part of the waveform data).

Power down sequence

- Open the VCOM switch.
- Disable source and gate outputs by SD_OE=GD_OE=0.
- Shut down the HV power supplies in the reverse order of Power up sequence and allow to go to 0V (GND) (Active discharge recommended).
- Disable VDD.

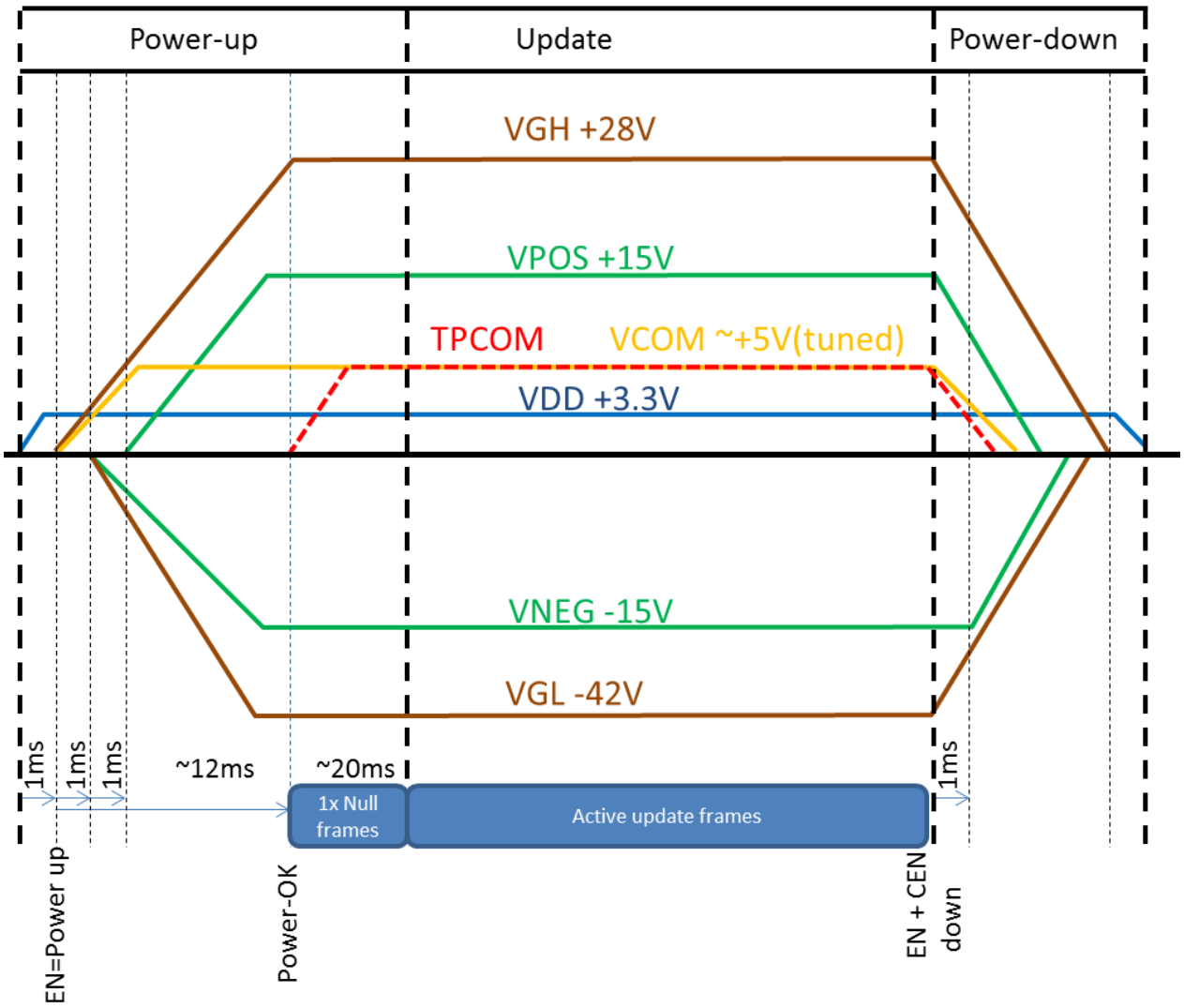

Figure 5: Power up/down sequence

5.4 AC Characteristics

For details of AC timing please also check driver chip datasheets.

6. Handling requirements

The display module is an electrostatic discharge (ESD) sensitive device. Ensure proper ESD precautions are in place to avoid damage to the display module.

The display module must be shipped in its unfolded flat state. All loose tails must be constrained during shipping.

Take appropriate care to protect the rear side of the display module from indents and punctures as this may damage the display. Take appropriate care to ensure the minimum bend radii of the flex tails are not violated (see Table 1).

In the application the gate and source driver chips must be protected from light to avoid unwanted drift effects.

7. Safety and Flammability requirements

The integrator of this display module into a final product is responsible for ensuring that the relevant safety and flammability requirements are met.